contact with the first HVNW region and the second HVNW region. An n-type buried well region is underlying the PBL. The p-well region and the n-type buried well region are in contact with a top surface and a bottom surface, respectively, of the PBL. The device further includes a n-well region in a top portion of the p-well region, an n-type source region in the n-well region, a gate stack overlapping a portion of the p-well region and a portion of the second HVNW region, and a channel region under the gate stack. The channel region interconnects the n-well region and the second HVNW region.

[0050] The foregoing outlines features of several embodiments so that those skilled in the art may better understand the aspects of the present disclosure. Those skilled in the art should appreciate that they may readily use the present disclosure as a basis for designing or modifying other processes and structures for carrying out the same purposes and/or achieving the same advantages of the embodiments introduced herein. Those skilled in the art should also realize that such equivalent constructions do not depart from the spirit and scope of the present disclosure, and that they may make various changes, substitutions, and alterations herein without departing from the spirit and scope of the present disclosure.

What is claimed is:

1. A device comprising:

a buried well region of a first conductivity type;

a first High-Voltage Well (HVW) region of the first conductivity type over the buried well region;

a first well region of a second conductivity type opposite to the first conductivity type, wherein the first well region comprises an edge contacting an edge of the first HVW region;

a drain region of the first conductivity type in a surface portion of the first HVW region;

a first source region of the first conductivity type in a surface portion of the first well region;

a first gate electrode over the first HVW region and the first well region, with the drain region and the first source region on opposite sides of the first gate electrode;

a plurality of buried regions of the second conductivity type, wherein the plurality of buried regions is parallel to each other, and is over and contacting a top surface of the buried well region; and

a plurality of HVW regions of the first conductivity type separating the plurality of buried regions from each other, wherein the plurality of buried regions and the plurality of HVW regions are spaced apart from the first source region by the first well region.

2. The device of claim **1** further comprising a second well region in an upper portion of the first well region, wherein the second well region is spaced apart from the plurality of buried regions and the plurality of HVW regions by a bottom portion of the first well region.

3. The device of claim **2**, wherein the second well region overlaps the plurality of buried regions and the plurality of HVW regions.

4. The device of claim **1** further comprising:

a second source region of the first conductivity type in an additional surface portion of the first well region, wherein the first source region and the second source region are spaced apart from each other by a portion of the first well region.

5. The device of claim **4** further comprising:

a second gate electrode overlapping the first well region, wherein the first gate electrode is electrically connected to the second gate electrode; and

a second HVW region with a portion overlapped by the second gate electrode, wherein the first HVW region and the second HVW region are on opposite sides of, and are connected by, the plurality of HVW regions, wherein the second HVW region is in contact with the buried well region.

6. The device of claim **4**, wherein the first source region and the second source region are electrically interconnected.

7. The device of claim **1** further comprising a pickup region of the second conductivity type in a top portion of the first well region.

8. A device comprising:

an n-type buried well region;

a first P-type Buried Layer (PBL) over and contacting the n-type buried well region;

a p-well region over and contacting the first PBL;

a first n-well region and a second n-well region in a top portion of the p-well region, wherein the first n-well region and the second n-well region are separated from each other by the p-well region;

a first n-type source region and a second n-type source region in the first n-well region and the second n-well region, respectively;

a first HVNW region and a second HVNW region contacting opposite edges of the p-well region;

a first gate stack overlapping a portion of the p-well region and a portion of the first HVNW region; and

a second gate stack overlapping a portion of the p-well region and a portion of the second HVNW region.

9. The device of claim **8** further comprising a drain region in the first HVNW region, wherein the first n-type source region, the second n-type source region, the first gate stack, and the second stack are comprised in a same Metal-Oxide-Semiconductor (MOS) device.

10. The device of claim **8**, wherein the first n-well region and the second n-well region are spaced apart from the first PBL by a bottom portion of the p-well region.

11. The device of claim **8** further comprising a third HVNW region over and contacting the n-type buried well region, wherein the third HVNW region connects the first HVNW region to the second HVNW region, and wherein the third HVNW region is spaced apart from the first n-well region and the second n-well region by a bottom portion of the p-well region.

12. The device of claim **11**, wherein the third HVNW region comprises an edge contacting an edge of the first PBL.

13. The device of claim **11** further comprising a second PBL, wherein the first PBL and the second PBL are in contact with opposite edges of the third HVNW region.

14. The device of claim **8** further comprising a heavily doped p-well pickup region between the first n-type source region and the second n-type source region.

15. The device of claim **8**, wherein the first n-type source region and the second n-type source region are electrically interconnected, and the first gate stack and the second gate stack are electrically interconnected.

16. The device of claim **8**, wherein the first HVNW region and the second HVNW region contact the n-type buried well region.